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EXAMINER
VITAL, PIERRE M

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/922,153	MORAN, DOV
	Examiner	Art Unit	
	Pierre M. Vital	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>07 September 2004</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1,3-30 and 36</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1,3-30 and 36</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>30 July 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____.

       3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Amendment

1.   This Office Action is in response to applicant's communication filed September 7, 2004 in response to PTO Office Action mailed May 15, 2004. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2.   Claims 1, 3-30 and 36 have been presented for examination in this application. In response to the last Office Action, no claims have been amended. No claims have been canceled. Claim 36 has been previously added. As a result, claims 1, 3-30 and 36 are now pending in this application.

3.   Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Response to Arguments

4.   Applicant's arguments with respect to claims 19, 22-28 and 36 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 1, 10-13, 16-18, 20-21 and 29-30 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Brown et al (US 6,201,739) and Kakinuma et al (US 5,640,349)

and further in view of Garner (US 6,549,482).

As per claims 1, 12, 18, 20 and 21, Brown discloses a flash-based unit for

providing code to be executed by an external processor that is in communication with

the flash based unit by a first bus, the flash based unit comprising a flash memory for

storing the code to be executed [*flash EPROM stores both code and data;* col. 9, line 50], said

flash memory being of a type such that the code cannot be executed in place from said

flash memory [*although a flash EPROM is used, NAND flash may be used as well;* col. 5, lines 30-

33]; a volatile memory component for receiving at least a portion of the code to be

executed, such that at least said portion of the code is executed by the external

processor from said volatile memory component [*the code of the flash memory is copied to

volatile memory where the processor can satisfy the code fetch request;* col. 4, lines 4-8].

However, although Brown discloses that the volatile memory and the flash

EPROM could be coupled to the processor via separate buses [col. 3, lines 64-65], the

reference does not specifically teach a logic, separate from the external processor, for

receiving command to move said at least portion of the code from said flash memory to

said volatile memory component; and a second bus, separate from said first bus,

whereby said logic moves said at least portion of the code from said flash memory to

said volatile memory component; and that a processor could execute code resident in

volatile memory as recited in the claims.

Kakinuma discloses a logic, separate from the external processor, for receiving

command to move said at least portion of the code from said flash memory to said

volatile memory component [*flash memory controller 2 controls read/write to/from flash memory*

based on command by host computer; Fig. 3, col. 1, line 35 – col. 2, line 3]; and a second bus,

separate from said first bus, whereby said logic moves said at least portion of the code

from said flash memory to said volatile memory component [*note that the flash memory 4*

communicates with S-RAM 3 and host 1 through a separate bus; Fig. 3].

Garner discloses a processor could execute code resident in volatile memory [*the*

code can be executed from RAM; col. 2, lines 30-34].

It would have been obvious to one of ordinary skill in the art, having the

teachings of Brown and Kakinuma and Garner before him at the time the invention was

made, to modify the system of Brown to include a logic, separate from the external

processor, and a separate bus for communication between the flash memory and the

volatile memory because a separate logic functions to control write/read operation

to/from a flash memory based upon a command by a host processor (Kakinuma, col. 1,

lines 35-37); using a separate bus is well known to benefit by improving system

throughput; and executing code resident in volatile memory is well known to benefit by

allowing the processor to perform an executable command instruction to the flash

device while reading the code from RAM (Garner, col. 2, lines 36-37).

As per claims 10 and 16, Brown discloses a volatile memory component selected

from the group consisting of SRAM or DRAM [col. 4, lines 1-3].

As per claim 11 and 17, Garner discloses the initialization code is boot code [col.

2, lines 38-42].

As per claim 13, Brown discloses a restricted non-volatile memory is a flash

memory [col. 5, lines 30-32].

As per claims 29 and 30, Brown discloses a port for providing to the external

processor said at least portion of the code received by said volatile memory component

[*port located between host computer 1 and host computer interface control 5*; Fig.3].

7.   Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Brown et al (US 6,201,739) and Kakinuma et al (US 5,640,349) and further in view of

Garner (US 6,549,482) and Anderson et al (US 6,295,577).

As per claim 3, the combination of Brown and Kakinuma and Garner discloses

the claimed invention as detailed above in the previous paragraphs. However, Brown

and Kakinuma and Garner do not specifically teach a power storage for storing at least

a limited amount of power for supplying power to the flash-based unit if power is not

otherwise available, power being drawn form said power storage when said logic

determines that said power is not otherwise available as recited in the claim.

Anderson discloses a power storage for storing at least a limited amount of

power for supplying power to the flash-based unit if power is not otherwise available,

power being drawn form said power storage when said logic determines that said power

is not otherwise available [*power is supplied to the non-volatile memory upon loss of power;* col. 6,

lines 2-6].

As per claim 4, the combination of Brown and Kakinuma and Garner discloses

the claimed invention as detailed above in the previous paragraphs. However, the

combination of Brown and Kakinuma and Garner does not specifically teach a power

storage providing only sufficient power to write data in said volatile memory to said flash

memory as recited in the claim.

Anderson discloses a power storage providing only sufficient power to write data in said volatile memory to said flash memory [*data is stored from volatile memory to non-volatile memory upon detection of loss of power;* col. 5, lines 61-67].

As per claim 5, the combination of Brown and Kakinuma and Garner discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Brown and Kakinuma and Garner does not specifically teach the power storage is a capacitor as recited in the claim.

Anderson discloses the power storage is a capacitor [col. 3, lines 62-63].

It would have been obvious to one of ordinary skill in the art, having the teachings of the combination of Brown and Kakinuma and Garner and Anderson before him at the time the invention was made, to modify the system of Brown and Kakinuma and Garner to include a power storage for storing at least a limited amount of power for supplying power to the flash-based unit if power is not otherwise available, power being drawn form said power storage when said logic determines that said power is not otherwise available; a power storage providing only sufficient power to write data in said volatile memory to said flash memory and the power storage is a capacitor because it would have decreased system cost by using a back EMF to power the non-volatile memory rather than battery based systems [col. 5, lines 10-14] as taught by Anderson.

8.   Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Brown et al (US 6,201,739) and Kakinuma et al (US 5,640,349) and further in view of

Garner (US 6,549,482) and Mills et al (US 6,385,688).

As per claims 6 and 7, the combination of Brown and Kakinuma and Garner

discloses the claimed invention as detailed above in the previous paragraphs. However,

the combination of Brown and Kakinuma and Garner does not specifically teach a single

chip or die for containing all components of a flash based unit as recited in the claims.

Mills discloses a single chip or die for containing all components of a flash based

unit [col. 20, lines 1-4].

It would have been obvious to one of ordinary skill in the art, having the

teachings of the combination of Brown and Kakinuma and Garner and Mills before him

at the time the invention was made, to modify the system of the combination of Brown

and Kakinuma and Garner to include a single chip or die for containing all components

of a flash based unit because it would have improved system performance by reducing

or eliminating the lengthy process of obtaining information from disk when power is

turned on [col. 9, lines 15-20] as taught by Mills.

9.   Claims 8-9 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Brown et al (US 6,201,739) and Kakinuma et al (US 5,640,349) and further in view

of Garner (US 6,549,482) and Nakata (US 6,523,101).

As per claims 8 and 14, the combination of Brown and Kakinuma and Garner

discloses the claimed invention as detailed above in the previous paragraphs. However,

the combination of Brown and Kakinuma and Garner does not specifically teach a flash

memory only permitting data to be read in one or more specific sizes of blocks as

recited in the claim.

Nakata discloses a flash memory only permitting data to be read in one or more

specific sizes of blocks [*ROM indicates copy size of initialization data to be stored into RAM;* col. 3,

lines 41-44].

It would have been obvious to one of ordinary skill in the art, having the

teachings of the combination of Brown and Kakinuma and Garner and Nakata before

him at the time the invention was made, to modify the system of the combination of

Brown and Kakinuma and Garner to include a flash memory only permitting data to be

read in one or more specific sizes of blocks because it would have increased execution

speed of the program by allowing the text codes stored on the ROM to be copied once

into the RAM [col. 1, lines 43-46] as taught by Nakata.

As per claims 9 and 15, Brown discloses a flash memory is a NAND-type flash

memory [*although a flash EPROM is used, NAND flash may be used as well;* col. 5, lines 30-33].

10.   Claims 19, 22-28 and 36 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Gefen et al (US PUB 2002/0138702) and Garfunkel (US 6,615,404).

As per claims 19, Gefen discloses a method for booting a system, the system

featuring a processor for executing boot code, the method comprising:

providing a flash based unit in the system for storing the boot code to be

executed [*NAND Flash 14; Fig. 1*], said flash-based unit comprising a flash memory of a

restricted type, being characterized in that code cannot be directly executed from said

flash memory [*NAND Flash is not executable*; Paragraph 8], and a volatile memory

component for receiving a portion of the boot code to be executed [*SRAM memory 10 and*

SRAM buffer 20; Figs. 1 and 2];

sending a busy signal to said processor (Paragraph 38);

transferring said portion of the boot code to said volatile memory component

(where it is understood that the system remains busy until the required data is

transferred; Paragraph 40);

removing said busy signal (where it is understood that once the required data is

transferred, other data requests can resume; Paragraphs 39-40).

However, Gefen does not specifically teach said portion of the boot code being

for basic initialization of the system and executing the portion of the code to boot the

system as recited in the claim.

Garfunkel discloses a portion of the boot code being for basic initialization of the

system (*initialization continues from RAM; a new downloading and programming process is enabled;*

column 7, lines 27-38); executing said first portion of the boot code by said processor to

boot the system (*the RAM enables the controller to operate the system;* column 4, lines 46-52).

Thus, it would have been obvious to one of ordinary skill in the art, at the time of

invention by applicant to modify the system of Gefen to include portion of boot code for

basic initialization of a system and executing the boot code to boot the system because

it was well known to enable the downloading process of a new initialization program and

operating software version during normal operation of a system (column 3, lines 23-25)

is well known to benefit by preventing reprogramming instruction errors.

As per claim 22, Gefen discloses a method for booting a system, the system

featuring a processor for executing boot code, the method comprising:

providing a flash based unit in the system for storing the boot code to be

executed (*NAND Flash 14; Fig. 1*), said flash-based unit comprising a flash memory of a

restricted type, being characterized in that code cannot be directly executed from said

flash memory (*NAND Flash is not executable;* Paragraph 8), and a volatile memory

component for receiving a portion of the boot code to be executed (*SRAM memory 10 and*

SRAM buffer 20; Figs. 1 and 2).

However, Gefen does not specifically teach said portion of the boot code being

for basic initialization of the system and containing a command for copying a second

portion of the code (*initialization continues from RAM; a new downloading and programming process*

is enabled; col. 7, lines 27-38); executing said first portion of the boot code by said

processor to boot the system (*the RAM enables the controller to operate the system*; col. 4, lines

46-52) as required in the claim.

Garfunkel discloses a portion of the boot code being for basic initialization of the

system and containing a command for copying a second portion of the code (*initialization*

continues from RAM; a new downloading and programming process is enabled; col. 7, lines 27-38);

executing said first portion of the boot code by said processor to boot the system (*the*

RAM enables the controller to operate the system; col. 4, lines 46-52).

Thus, it would have been obvious to one of ordinary skill in the art, at the time of

invention by applicant to modify the system of Gefen to include portion of boot code for

basic initialization of a system and executing the boot code to boot the system because

it was well known to enable the downloading process of a new initialization program and

operating software version during normal operation of a system (column 3, lines 23-25).

Claim 23 is rejected using the same rationale as for the rejection of claim 22

above. Garfunkel further discloses transferring a second portion of the code to said

volatile memory component for booting the system (col. 7, lines 27-38).

As per claim 36, Garfunkel discloses a flash-based unit separate from the

processor (*flash memory 12 is separate from processor coupled to comm. link 14*; Fig. 1; col. 7,

lines 62-66).

As per claims 24-28, Gefen and Garfunkel disclose the claimed invention as

detailed per claim 22 above in the previous paragraphs.

Gefen further discloses a volatile memory is large enough to store portion of the

boot code only sufficient for basic initialization of a system (the NAND Flash is 8mB

while the SRAM is 1KB, equal or smaller in size to the portion of code in the flash

memory; Paragraph 30).

11.   Claims 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Brown et al (US 6,201,739) and Kakinuma et al (US 5,640,349) and further in view of

Garfunkel et al (US 6,615,404).

As per claims 31-35, Brown discloses a flash-based unit for providing code to be

executed by an external processor that is in communication with the flash based unit by

bus, the flash based unit comprising a flash memory for storing the code to be executed

[*flash EPROM stores both code and data;* col. 9, line 50], said flash memory being of a type

such that the code cannot be executed in place from said flash memory [*although a flash*

EPROM is used, NAND flash may be used as well; col. 5, lines 30-33]; a volatile memory

component for receiving at least a portion of the code to be executed, such that at least

said portion of the code is executed by the external processor from said volatile memory

component [*the code of the flash memory is copied to volatile memory where the processor can satisfy*

the code fetch request; col. 4, lines 4-8].

However, Brown does not specifically teach a logic, separate from the external

processor, for receiving command to move said at least portion of the code from said

flash memory to said volatile memory component upon receipt of a power-on signal as

recited in the claim.

Kakinuma discloses a logic, separate from the external processor, for receiving

command to move said at least portion of the code from said flash memory to said

volatile memory component [*flash memory controller 2 controls read/write to/from flash memory based on command by host computer*; Fig. 1A, 1B, col. 1, line 35 – col. 2, line 3]. Since the technology for implementing a logic separate from a processor for moving data was well known, and since a separate logic functions to control write/read operation to/from a flash memory based upon a command by a host processor, an artisan would have been motivated to implement a logic separate from a processor in the system of Brown.

However Kakinuma does not specifically teach the use of a power-on signal to move code data from said flash memory to said volatile memory component as recited in the claim.

Garfunkel discloses moving code data from a flash memory to a volatile memory component upon power-on [col. 5, lines 12-15]. Since the technology for implementing moving code data from a flash memory to a volatile memory component upon power-on was well known, and since moving code data from a flash memory to a volatile memory component upon power-on eliminates a situation where the flash memory contains only corrupted or incomplete software version, an artisan would have been motivated to implement moving code data from a flash memory to a volatile memory component upon power-on in the system of Brown and Kakinuma.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a logic separate from a processor for moving data, because a logic

separate from a processor was well known to benefit by control write/read operation

to/from a flash memory based upon a command by a host processor as taught by

Kakinuma; and to move code data from a flash memory to a volatile memory

component upon power-on, because move code data from a flash memory to a volatile

memory component upon power-on was well known to benefit by eliminating a situation

where the flash memory contains only corrupted or incomplete software version as

taught by Garfunkel.

Conclusion

12.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider

these references fully when responding to this action. The documents cited therein

teach non-executable flash memory.

13.   The examiner requests, in response to this Office action, support be shown for

language added to any original claims on amendment and any new claims. That is,

indicate support for newly added claim language by specifically pointing to page(s) and

line no(s) in the specification and/or drawing figure(s). This will assist the examiner in

prosecuting the application.

14.   When responding to this office action, Applicant is advised to clearly point out the

patentable novelty which he or she thinks the claims present, in view of the state of the

art disclosed by the references cited or the objections made. He or she must also show

how the amendments avoid such references or objections See 37 CFR 1.111(c).

15.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Pierre M. Vital whose telephone number is (571) 272-

4215. The examiner can normally be reached on 8:30 am - 6:00 pm, alternate Fridays

off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

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Business Center (EBC) at 866-217-9197 (toll-free).

May 17, 2006

PIERRE VITAL
PRIMARY EXAMINER